**IN THE SPECIFICATION**

Please amend the specification as provided below:

Please amend the paragraph beginning on page 7, line 16 as follows:

Referring to Fig. 1 of the drawing, high speed communication system 1 consists of a transmitter 10 interconnected by a transmission facility 12 with a receiver 11. Information is transmitted to receiver 11 by transmitter 10 in a binary coded pulse format as a high speed binary pulse bit stream 13 applied to the input of transmission facility 12. Transmission facility 12 may be any one of a large number of high speed transmission facilities such as printed circuit traces, coaxial cables, optical fibers, radio and satellite links or the like. In a typical application, the binary pulses of input binary bit stream 13 may be reconfigured by the characteristics of the transmission facility 12 and appear as the rounded binary coded pulse format shown as the binary bit stream 14 received by receiver 11. The binary pulse coded waveform measuring apparatus may be connected to transmission facility 12 at either the output of transmitter 10, the input of receiver 11, at various locations along transmission facility 12 or at various locations within transmitter 10 and receiver 11 wherein it is desired to measure the quality and characteristics of the transmitted and received binary pulse coded bit streams 13 and 14. In operation, control apparatus 3 controls the operation of count logic 2 to generate an eye diagram representing the quality characteristics of the measured ~~the~~ binary pulse coded bit streams 13 and 14 on display apparatus 4 which may be any one of a number of well known display devices such as a computer, stand alone monitors, plotters, various storage devices, work stations or the like. The configuration of the eye diagram displayed on ~~monitor~~ the display apparatus 4 shows the characteristics of the measured binary pulse bit stream.

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Please amend the paragraph beginning on page 8, line 15 as follows:

In general, a binary pulse coded bit stream consists of a series of succeeding "0" and "1" pulses wherein each "0" pulse is transmitted at one voltage level and each "1" pulse is transmitted at another voltage level. The specific sequence of the ~~of the~~ "0" and "1" pulses define the information or data transmitted by transmitter 10 to receiver 11. The pulses have a repetition rate wherein each pulse has a period of time, hereinafter referred to as the pulse period, and follows a preceding pulse at the repetition rate determined by the communication system clock. In an exemplary embodiment of the invention, an apparatus in accordance with the invention for measuring the characteristics of the bit stream of binary pulses 13, 14 has control apparatus 3 for defining a window comparator. Control apparatus 3 may be a computer, processor, work station, or the like, the details of which are well known, and which is specifically programmed or configured to establish an array, Fig. 3, of columns and rows defining the points for accumulating event counts at time offsets during the defined durations of the measured binary pulse bit stream. Data collected from the measured waveform of the binary pulse bit stream is accumulated at each column and row location, hereinafter called points, for a defined duration of a part of the binary pulse bit stream. The accumulated data is then drawn as an eye diagram, Fig. 1, on ~~monitor~~ the display apparatus 4 to define characteristics of the binary pulse bit streams 13 and 14.

Please amend the paragraph beginning on page 9, line 10 as follows:

Control apparatus 3, Fig. 1, is programmed to create a voltage threshold window that moves between a minimum voltage threshold $V_{MIN}$ and a maximum voltage threshold $V_{MAX}$ with row changes of the array and which has an incremental voltage $\Delta V$ difference equal to the value of ($V_{MIN}$ - $V_{MAX}$) divided by the maximum number of rows in the array. Count logic apparatus 2 detects voltage levels of the binary pulses occurring

at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window and accumulates the counts during the duration times at each row and column point of the array. In particular, control apparatus 3, Fig. 2, applies a value of voltage V+ ΔV, 200, to the ~~plus~~ positive input of comparator 202 and a value of voltage V, 201, to the ~~minus~~ negative input of comparator 203 to create a voltage threshold window. The count logic apparatus 2 responds to a signal occurring during the duration of a part of the binary pulse bit stream by detecting the voltage level of a pulse at time offset and determines if the measured pulse voltage level is within the threshold levels defined by the window comparator of the array. When the measured pulse voltage level is below the threshold voltage level V + ΔV, comparator 202 operates to set logic device 204. If the measured pulse voltage level is above the threshold voltage level V, comparator 203 operates to set logic device ~~203~~ 205. The setting of logic devices 204 and 205 enable AND gate 206 to indicate that the measured pulse level is within the voltage threshold window between the value of V and V + ΔV for each column and row of the array. Logic counter 207 accumulates counts of the detected binary pulse voltage levels within the voltage threshold window at time offsets during each duration part of the binary pulse bit stream in a column and row point of the array.

**IN THE CLAIMS**

Please amend the claims to read as shown below:

1. (Original) Apparatus for measuring characteristics of a bit stream of binary pulses comprising:

control means for defining a window comparator, and

logic means for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics.